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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,917	09/22/2003	Kenichi Imamiya	002372.00047	5120
22907	7590	03/30/2004	EXAMINER	
BANNER & WITCOFF 1001 G STREET N W SUITE 1100 WASHINGTON, DC 20001			CUNNINGHAM, TERRY D	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/664,917

Applicant(s)

IMAMIYA, KENICHI

Examiner

Terry D. Cunningham

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 September 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☒ Certified copies of the priority documents have been received in Application No. 09/863,408.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>09222003</u> . | 6) <input type="checkbox"/> Other: ____  |

## **DETAILED ACTION**

### ***Drawings***

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, timing diagrams showing an overlapping period when the “first capacitors” and the “second capacitors” are being charged (as discussed above) and a period wherein the “NMOS transistor” of the “first transfer device” and/or the “second transistor device” is “turned on during a period in which the first and the second period overlap” (as discussed below) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-5 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification fails to enable the present invention with respect to the “overlapping portions” of the charging phases. All that is found regarding this operation is the discussion in paragraph 17 on page 7. This section states that “the second capacitors being charged during a second period the partially overlaps with the first period”. However, there is no other discussion whatsoever found for this operation in the specification. Additionally, the operation is not seen to be consistent the elected embodiment in Figs. 16-17. As understood, the capacitors C1

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charged (i.e., the charging periods) when the corresponding signal  $\phi 1$  and  $\phi 2$  are low. There is no overlapping period found in the Fig. 17 wherein both signals  $\phi 1$  and  $\phi 2$  are low at the same time.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is not understood how the disclosed circuit can operate, similarly as discussed above.

Claims 2-5 are rejected for the reasons discussed above with claim 1.

In claim 2, lines 9-10, there is no support found in the specification for the “NMOS transistor” being “turned on during a period in which the first and the second period overlap each other”. As discussed above, there is no period found in Fig. 17 wherein the “first and the second period overlap each other”, thus it is not seen that the “NMOS transistor” can turn on during this period.

Claim 3 is rejected for similar reason as claim 2.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 4 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Bloch et al. (USPN 6,130,574). Bloch et al. disclose, in Fig. 3, a circuit comprising: "a plurality of first capacitors (Cp1 - CpN, odd)"; "a plurality of second capacitors (Cp1 - CpN, even)"; "a first transfer device (Tx2)"; and "a second transfer device (Tx3)", all connected and operating similarly as recited by Applicant.

Claims 1-5, insofar as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Li et al. (USPN 6,373,324). Li et al. disclose, in Figs. 1-2, a circuit comprising: "a plurality of first capacitors (Cp1 - CpN, odd)"; "a plurality of second capacitors (Cp1 - CpN, even)"; "a first transfer device (Tx2)" having "a first NMOS transistor (132)"; "a second transfer device (Tx3)" having "a first NMOS transistor (133)"; "a third capacitor (140 or 141)" and "a second NMOS transistor (143 or 144)", having, all connected and operating similarly as recited by Applicant. Examiner notes that the timing diagrams of Li et al. are similar to the of Applicant's Fig. 17.

***Conclusion***


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terry Cunningham whose telephone number is 571-272-1742.

The examiner can normally be reached on Monday-Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TC  
March 22, 2004

  
Terry D. Cunningham  
Primary Examiner  
Art Unit 2816